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09/301,284	04/28/1999	SHUICHI TAKAYAMA	NAK1-BG86	5392

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Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Applicati n No. 09/301,284	Applicant(s) TAKAYAMA ET AL.
	Examiner Ted T. Vo	Art Unit 2122

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003* .

2a)☒ This action is FINAL. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,49 and 50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,49 and 50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *22* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the communication filed on 7/11/2003.

Claims 1 and 49 are amended. Claim 50 is added. Claims 1-11, and 49-50 are pending in the application.

Response to Amendments

2. With regards to the amendment and the illustration given in the remarks, the objection to the specification is withdrawn; the rejection of 35 U.S.C. 112, second paragraph is withdrawn.
-The issue of 35 U.S.C. 112, first paragraph in prior action regards the limitation "*the processing packet being made of an integer number of bytes*", which is deleted in the current amendment of the claim 1, page 2, line 10, and of claim 49, page 6, line 18. The issue regards the limitation (which was deleted) broadening an arbitrary number that lacks support in the specification.
However, the limitation regarding this issue is reenter in the newly added limitation of claim 1 and 49 as "*at least one processing packet being made of an integer number of bytes*", and "*the number of processing target instructions being any number except a power of 2*". As a result, the issue of 35 U.S.C. 112, first paragraph in prior action has never been resolved. Thus, the rejection of 35 U.S.C. 112 first paragraphs is maintained as directly to the newly added limitations.
See the action of this issue in the section 4 below.

Response to Arguments

3. Applicants' arguments have been considered. However the arguments are not persuasive.

a. Regarding the applicant's argument that Christie does not disclose, or teach the second program number by using the same number of values as the processing target instruction and cycling through the values as in the claim 1 and 49. Based on this argument, applicants conclude that Christie

does not disclose or suggest how to provide a program counter when the number of processing target instructions is a number other than power of 2.

Examiner respectfully responds: Applicants' amendment includes following recitations, "*at least one processing packet being made of an integer number of bytes*" and "*the number of processing target instructions being any number except for power of 2*". By amending these limitations, applicants broaden their processing target instructions within 0, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15, 17, etc.

-First, the 0 is included in the claim limitation. The number zero of processing target instructions makes very abstract to current known technology. With the number 0, it is not necessary to implement a counter.

-Second, the amended "*except for power of 2*" is an indented use. It aims to exclude the number of its processing target instructions from the four-byte instruction used in RISC processor.

In term of an integer number of processing target instructions, claims include an arbitrary number of a counter. The claimed functionality and the four-bit counter (Christie) do the same. They both address to an instruction packet.

Numerous Court decisions have analyzed the content of various claim language for meaningful, useful differences in structure or acts performed between the claims and the prior art. Some of these decisions have directed to an intended uses of a claim language.

See MPEP In re Schreiber, 128 F.3d 1473, 44 USPQ2d 1429 (Fed. Cir. 1997), the court affirmed a finding that a prior patent to a conical spout used primarily to dispense oil from an oil can inherently performed the functions recited in applicant's claim to a conical container top for dispensing popped popcorn. An examiner had asserted inherency based on the **structural similarity** between the patented spout and applicant's disclosed top, i.e., both structures had the same general shape. The court stated:

Nothing in Schreiber's [applicant's] claim suggests that Schreiber's container is of a different shape' than Harz's [patent]. In fact, [ ] an embodiment according to Harz (Fig. 5) and the embodiment depicted in Fig. 1 of Schreiber's application have the same general shape. For that reason, the examiner was justified in concluding that the opening of a conically shaped top as disclosed by Harz is inherently of a

size sufficient to allow [ ] several kernels of popped popcorn to pass through at the same time' and that the taper of Harz's conically shaped top is inherently of such a shape as to by itself jam up the popped popcorn before the end of the cone and permit the dispensing of only a few kernels at a shake of a package when the top is mounted to the container.'

In this subject matter, the claims' recitation against the prior art is in term of a number of processing target instructions.

Claiming of *"the number of processing target instructions being any number except for power of 2"* and Christie's least significant 4 bits of a potential next decode program counter are **structural similarity**.

In this subject matter, the claims tend to exclude the 4-bit decoded counter, 8-bit decoded counter, etc.; however, its functionality does not make structure dissimilarity from the prior art.

- In response to the argument that Christie does not disclose, or teach the second program number by using the same number of values as the processing target instruction and cycling through the values as in the claim 1 and 49.

Applicants' specification indicates a counter of three-bit counter circling through the same values of 000, 010, 100, where value 000 for the first processing target instruction, 010 for the second processing target instruction, and 100 for the third processing target instruction for m=3.

Christie generally says using four bits of a next decode program counter value to a ROP from the queue. When Christie expresses the term decoding, it means using the same value of a counter to decode to each ROP's position since the hardware logic cannot be varied. The fact is there are at least four values of Christie's counter connecting to four packets of the ROP in the instruction queue. In the same manner, there are at least three values of applicants' counter connecting to the processing target instructions. The two expressions are doing the same functionality. The different bit or the difference of counter connecting between the three-byte instructions and four byte instructions is only the implementation or intended use.

b. Regarding the applicant's argument that Christie fails to reliably specify a position of a next target instruction.

Examiner responds: The term "next decoder program counter value" (column 18, lines 8-11) corresponds an incrementing. Christie shows the incrementer 760 to increment the more significant counter (column 18, lines 26-27). Incrementing of a counter depends on processor execution. In other words, a prior art does not necessarily describe how to advance to a next instruction.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-11, 49-50 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

-Since the claims are claiming a utility of processing packet made of by an integer number of bytes. This arbitrary integer number corresponds to a packet of instructions arranged in memory storage and counted by a counter. A skill in the art, Christie, has disclosed a limit of m=4 byte-instructions (RISC) or a limited number of instructions for CISC. Another skill in the art, Engblom (Submitted herein) discusses a difficulty encountered in hardware design of a real-time processor in term of timing (see Engblom, section 4 Summary and Recommendation). The discussions of skills in the art show that timing is a constraint that limits the increase in size of memory and of counter. It is known in the art that a circuit element such as counter or adder has carry logics propagating through its bits. An increasing of bit numbers must account for timing analysis. In this subject matter, the claim recitations "*at least one processing packet being made of an integer mummer of bytes*" and "*the number of processing target instructions being any number except for power of 2*" with respect claim 1 and claim 49, and *"the number of the plurality of target instructions is equal to m where m is a number other than a number equal to 2**n",* with respect claim 50, lack utilities to support. The specification, discusses a hardware element of 3-bit counter to

position a packet of processing target instructions. The claims recite an arbitrary number m in which skills in the art shows hardly to implement. The lack in utilities for supporting a large number would make the disclosure not be enabled.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1-11, 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Christie et al., US Patent No. 5,559,975.

As per claim 1:

-Regarding claim limitations:

"*A processor for reading instructions from a memory according to a program counter, and for executing the read instructions,*

the memory storing (see column 7, lines 33-49, queue), *in a position corresponding to a byte boundary* (see column 7, lines 33-49, ROP), *at least one processing packet being made of an integer number of bytes, the processing packet including processing target instructions, each processing target instruction being an operation to be executed by the processor* (see column 18, lines 4-24, least significant four bits), *the number of processing target instructions being any number except for power of 2,*

the program counter including a first program counter and a second program counter (see column 18, lines 4-38, less significant program counter, and more significant program counter),

the first program counter indicating a storage position of the processing packet in the memory (see column 18, lines 24-38, more significant program counter),

the second program counter indicating a position of processing target instruction in the processing packet (see column 18, lines 4-23, less program counter) *by using the same number of values as the number of processing target instructions, and cycling through the values"* (see column 18, lines 4-11, least significant four bits of a potential next decode program counter),

Christie's reference teaches the less significant four bits program counter that provides least significant four bits of a potential next decode program counter to correspond to 4-bype ROP from program queue (see column 18, lines 4-11, least significant four bits of a potential next decode program counter), Christie uses (4:31) bits (*first program counter*), named as more significant program counter to position to a byte boundary of a RISC instruction set or a X86 instruction. The less significant program counter, which provides least significant four bits of a potential next decode program counter, and the more significant program counter increment or branch to the next instruction within a ROP or queue of RISC or X86 according to the processor.

Christie discloses the less significant program counter of four bits corresponding to a four-byte ROP instruction. The number of processing target instructions in ROP, 4, is not power of 2.

However, the difference is only the exclusive number of implementation, where the number is conforming to standards in size in accordance to the length of a given instruction set.

Therefore, it would be obvious to an ordinary skill in the art when performing counting of an instruction set in which the length of the set is not power of 2, would modify the counter in a **structural similarity**. Doing so would correspond to the number of instructions required by a given instruction set.

As per claims 49-50: Claims 49 and 50 have the functionality corresponding to the claim 1. Claims 49-50 are rejected in the same reason as set forth in connecting to the rejection of claim 1.

As per claim 2:

-Regarding claim limitations of claim 2, Christie teaches further claim limitations "first program counter updating and second program counter updating" using the incrementer, adders, and multiplexers (see column 18, lines 4-23, and lines 24-38).

As per claim 3:

-Regarding claim limitations of claim 3, claim 3 is inherent from relative address values used in a program when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38) to perform adding that sets the address of the relative address value in the program counters. To perform the adding a relative value included in an instruction, Christie discloses that in a branch, an instruction is fetched and decoded. The counter identifies the next address of the target instruction, and uses adders, selectors, to form the next address (this mechanism is provided in the discussion column 18, lines 4-38).

As per claim 4:

-Regarding claim limitations of claim 4, claim 4 manipulates a calculation performed by adders in the first counter in the second counter. Christie teaches the adding mechanism by showing the circuit of figure 9A, discussing branch (see column 2, lines 46-59), and discussing adding mechanisms (see column 18, lines 4-38).

As per claim 5:

-Regarding claim limitations of claim 5, claim 5 manipulates a calculation performed by adders in the first counter in the second counter corresponding to the functionality of claim 4. Christie teaches the adding mechanism by showing the circuit of figure 9A, discussing branch (see column 2, lines 46-59), and discussing adding mechanisms (see column 18, lines 4-38).

As per claim 6:

-Regarding claim limitations of claim 6, claim 6 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 7:

-Regarding claim limitations of claim 7, claim 7 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in

'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 8:

-Regarding claim limitations of claim 8, claim 8 is inherent from adding mechanism when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 9:

-Regarding claim limitations of claim 9, claim 9 is inherent from relative address values. It is rendered by a true principle and manipulated by add/subtract operations based on address values appeared in a microprogram when a branch address is taken (see column 2, lines 46-59). Christie's reference includes adders and multiplexers in 'more significant program counter portion' and 'less significant program counter portion' (see column 18, lines 4-38).

As per claim 10:

-Regarding claim limitations of claim 10, given the broadest interpretation of the claim in light of specification, Christie's processing packet is ROP which has a length number 4. Christie discloses the program counter (4:30) that is more significant than 4, the length of ROP.

As per claim 11:

-Regarding claim limitations of claim 11, functionality claim 11 is inherent in registers, read/write address buffers, cache, and fetch mechanism used to store data as shown in Christie's figures (Figures 1A...).

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. in the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (703) 308-9049. The examiner can normally be reached on Monday-Friday from 8:00 AM to 5:30 PM ET. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam, can be reached on (703) 305-4552.

The fax phone numbers for this Group are:

Official: (703) 746-7239.

After Final: (703) 746-7238.

Non-Official: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

TTV
September 22, 2003

ANTONY NGUYEN-BA
PRIMARY EXAMINER